

Trends in PM Chip Integration

Foundry-based integrated power management platforms

Power management electronic circuits have been around for decades. In recent years, two simultaneous trends are observed: Silicon power technology platforms are moving to the 0.18 micron node aggregating many design blocks on the same chip, and at the same time, production of these platforms is increasingly being outsourced from Integrated Device Manufacturers (IDMS) to foundries.

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The dual trend of chip integration and outsourcing the production of the silicon platform is more complex in power management platforms than it has been for RFICs and mixed-signal technologies. In power management platforms, device performance metrics such as specific R_{dson} vs. the safe operating area (SOA) may vary greatly between platforms produced on the same toolset. Low specific R_{dson} achieved by good device design may reduce chip size, a feat which in digital circuits requires migrating to a more advanced technology node and silicon production toolset. Other aspects such as latchup immunity and ESD protection may also depend on a clever design of the platform. Thus differentiation prevails over standardization, driven by expertise of the device and process teams more than it is by the equipment manufacturers. Foundries often enter this field bringing with them experience in the production of the base CMOS platform while importing the knowledge of the power platform from an IDM. This results with a specific platform which can address the needs of that single IDM. Such an offering may be very application-specific and at times is limited by exclusivity to a single customer for up to a lifetime. Thus foundries face the challenge to come up with a flexible offering which can serve a broad range of customers (less and more experienced) and applications (different voltages, analog and digital content and varying immunity to latchup and ESD) and serve as a starting point for custom designs.

Described here is a power management platform which addresses the broad needs of voltages of up to 80V breakdown and allows optimization of all power needs with the proper process complexity tradeoff.

Process Simplicity and Flexibility

Simplicity

Typically, power platforms that have been developed at IDMs are based on bipolar processes incorporating epitaxial growth and buried layers. Such structures allow high immunity to latchup and electrostatic discharge events. However, such processes consist of a large number of processing steps which renders the process complex, costly, and not always in tune with the requirements of all applications. The TowerJazz TS18PM/35PM process family utilizes a non EPI base platform and requires 4 additional layers to implement a process with voltages of up to 60V BV. Overall, for a 31m process, this platform requires 20 masks for a 5V gate process keeping the process complexity to a minimum. A buck converter technology demonstrator shows the platform operating at 2 amperes with no latchup issues.

Flexibility

While the platform has a simple process starting point, more complex process options need to be addressed for high end applications. The integration of very high density logic can be implemented by the addition of the 0.18 micron (1.8V) devices at the cost of 5 masks. This allows a high logic density (up to 125 Kgate/mm²) power management process, TS18PM at 25 masks (31m). Thus two process technology nodes TS18PM/35PM, are served by the same design kit family.

As there is a tradeoff between breakdown voltage and the specific on resistance (R_{dson}), the kit allows full flexibility in choosing the required breakdown voltage / specific R_{dson} tradeoff thus minimizing the area taken by the devices. The power devices are offered in 0.5V steps in operating voltage which are selectable in the kit menu (Figure 1).

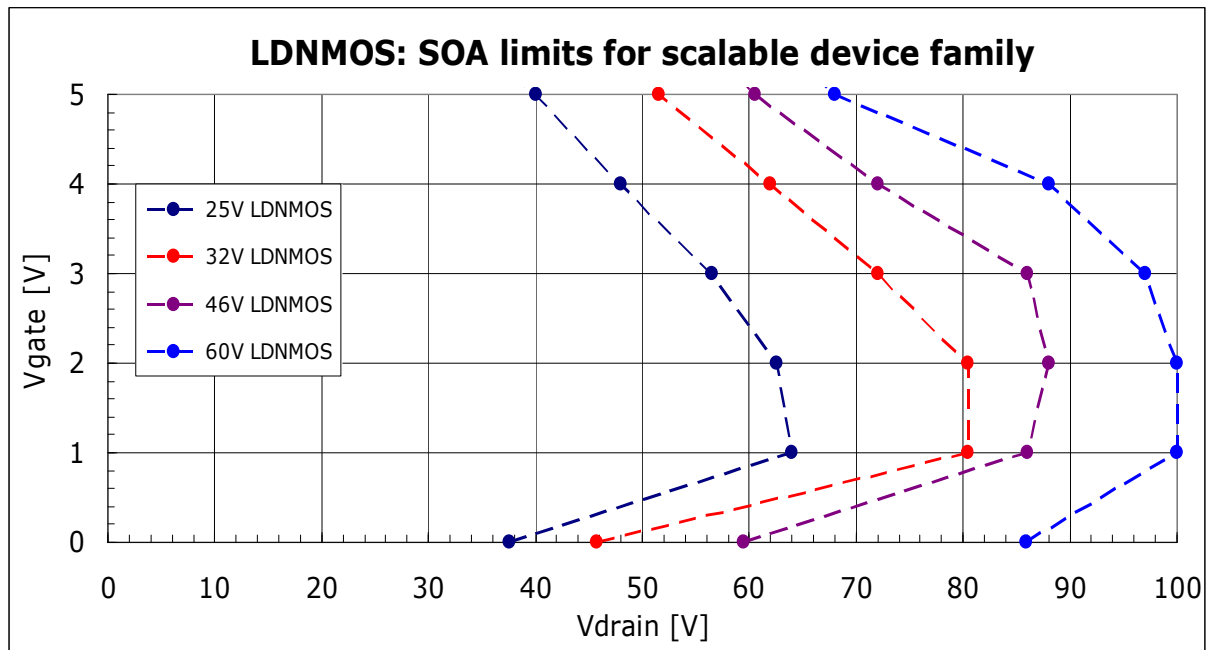
Safe operating area (SOA) curves (Figure 2) allow the selection of the right device depending on the switching waveforms. The selection of an ESD solution can also be made based on the knowledge of the SOA.

Figure 1: Selection graphic users interface for the power device in the PDK. The GUI allows a flexible selection of Guard Rings, Parasitic metal resistance calculation and self-heating effects.

Cell Name	nld_5v_sclV	off
View Name	symbol	off
Instance Name	M0	off

CDF Parameter	Value	Display
Cell Name	nld_5v_sclV	off
Finger Width (w)	5.0	off
Gate Length (l)	1.3	off
Columns Number (nc)	2	off
Rows Number (nr)	1	off
Calculate param	Max Vds Est	off
Source to Gate Space (S)	4.2	off
Max Vds Estimate	60.0 V	off
Max BVds Estimate	79.41636 V	off
Include Metal Parasitics?	<input checked="" type="checkbox"/>	off
Metal Resistance (Rm)	0.5505455	off
Ron Estimate	670.8236 Ohms	off
Thermal Resistance Option'	<input type="checkbox"/>	off
Metal Routing Level	M2	off
Connet Gate Rows By M2	<input checked="" type="radio"/> No <input type="radio"/> Left <input type="radio"/> Right <input type="radio"/> Both	off
Add Psub Ring	<input type="radio"/> No <input checked="" type="radio"/> PM <input type="radio"/> Tap	off
PM Guard Ring Number	1	off
AA Drain Width	1.1	off
Body Tie Width	0.54	off
WTN to Psub Diode Width	21.54	off
WTN to Psub Diode Length	12.2	off

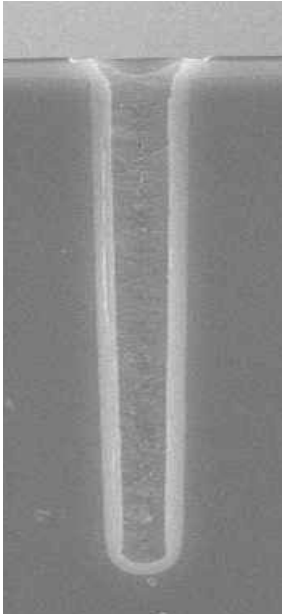
Figure 2: Safe operating area (SOA) graph and modes of operation. The allowed operating area is to the left of the curve. Depending on the switching curve, the proper device geometry may be selected featuring the right tradeoff for the value of the specific $R_{ds(on)}$ and SOA. The thick Blue line depicts a switching curve between on and off which stays away from the snapback point (high gate voltage, source drain voltage limit of the SOA).



Latchup immunity and isolation

Current injection to the substrate in integrated Power IC platforms is the most severe problem as compared between various IC platforms due to the high current levels of several amperes that integrated power may draw from the substrate. Consequently, positive feedback between any two (parasitic) bipolar transistors may lead to latchup and functional failures of the circuit. Remedies to this increased latchup sensitivity begin with a characterization of possible latchup paths and a definition of design rule recommendations. These design rule recommendations are supported by Process Design Kit (PDK) tools, Design Rule Check (DRC) decks that support them, automated guard ring configurations, options of use of epitaxial starting material, deep trenches (Figure 3) and buried layers.

Figure 3: Deep trench isolation may be incorporated as part of the power platform. The deep trench composed of oxide and polysilicon, isolates adjacent devices preventing latchup by cutting off bipolar positive feedback loops. It also allows denser spacing of devices.



All of these constitute a solution which may incur high process complexity. A flexible platform needs to offer optional use of the toolbox to attack latchup problems. At times, guard rings themselves may be the source of catastrophic latchup when they are on the ESD path. To make the path as robust as possible, an automated path for the layout of ESD and latchup structures is defined. An example of such a guard ring offering tool can be found in the selection menu of Figure 1.

ESD solutions

ESD solutions typically operate in two ways: RC detection and voltage triggering. Voltage triggered devices operate on the straightforward notion that above a certain voltage, the ESD device needs to open and allow current flow to ground, bypassing the circuit components and protecting them from damage. To operate in a robust manner, a margin needs to be kept for operating ESD devices. The ESD device trigger voltage needs to be between the operating voltage and the destructive voltage of the device, with enough margins to account for process and power supply variations. A power management platform optimizes its window so that the protected power devices need not handle unnecessary higher voltages as this would cost in higher specific R_{dson} and hence circuit area.

To bypass the design window R_{dson} tradeoff limit, RC detect circuits may be employed. These circuits are triggered by the fast rise in the voltage or current of the ESD pulse and hence need not fit a static ESD design window. However, the designer needs to be careful that the environment they are in is not subject to inductive spikes that can trigger the device. To maintain full flexibility of an ESD package, TowerJazz therefore employs in its roadmap two solutions: RC detect and voltage triggered devices. The selection of an ESD solution can be made based on the knowledge of the SOA provided with the kit (Figure 2).

Optimized R_{dson} for a wide voltage range, modeling

Specific R_{dson} is optimized by using amongst other things self aligned implants. A scalable model and pcell set are implemented to allow the optimization of R_{dson} for any given voltage need. The SOA is mapped so that for a given application the optimum switching conditions may be selected (Figure 2). In switching applications, the device toggles between high source drain voltage at zero gate voltage (“off state”) and low drain voltage high gate voltage (“on state”). To be able to make use of SOA optimization, designers need to know that the modeling can allow accurate dynamic tracking of the device performance. For example, knowing that inductive spikes would not take them past the SOA in the high gate voltage high source drain voltage region which otherwise is seldom accessed. Knowledge of the details of the SOA backed by good dynamic modeling allows the designer to extend device performance further achieving a better specific R_{dson} –Breakdown voltage trade off than a basic conservative square SOA definition allows. Good dynamic and capacitive modeling also allows modeling of the switching characteristics of the device, a key factor in designing efficient switching converters. To address the above, the TS18PM/35PM employs a voltage scalable device model which covers all the power device offering in the kit. The model accurately accounts for the device parasitics and simulates accordingly the switching characteristics of the power devices. Added features include self heating effects and metal parasitic resistance calculations.

Digital NVM

Power applications require some non-volatile memory (NVM) starting from “fuse like” one time programmable (OTP) memories needed for trimming applications to applications that have more digital content and require code storage. Classical embedded NVM solutions require many masks and complicate the process. In recent years, solutions called “Digital NVM” which require

little or no process modifications to the CMOS platform have been introduced. TowerJazz has introduced such solutions (Cflash) to RFID platforms which necessitate low mask count. TowerJazz's Cflash solution follows the cell size needed (10s micron²) for RFID solution with low power consumption. Some power applications require denser flash and hence require a smaller cell size. TowerJazz, relying on its experience in developing flash cell technology, has developed a smaller size "Digital NVM" (Yflash) unit cell of 3 micron².¹ In addition to its small cell size, the Yflash solution is adapted to using 5V gate oxides which are implemented in Power Management Platforms.

Analog and Digital Offering

The base platform, a foundry's core knowledge, includes a full analog offering ranging from statistical mismatch models for all components and a full analog offering. Rich IP coverage for the digital and analog platforms is available on the base platform. The TowerJazz Platform utilizes a 0.18 micron and a hybrid 0.5 micron (front end) / 0.18micron (backend) base CMOS analog platform for its TS18PM/35PM power management process family. The base platforms utilized have a long history of usage and come with a rich analog device, modeling, and digital-analog IP offering.

The platforms described above are the result of TowerJazz's efforts to address the diverse needs of the power management design community. As described, the solution provided by a foundry may differ in style from an internal IDM solution.

As integrated power management platforms continue to migrate to foundries, more flexible solutions will be offered by these foundries. In many cases the ease of use flexibility and performance will determine their success rather than standardization.

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