

GSA Mixed-Signal/RF Subcommittee Is Facilitating an Analog Ecosystem

By Marco Racanelli

Outsourcing the manufacturing for analog technology is creating a new supply chain. It also is supporting an ecosystem that mirrors the already well-established method that's used for digital technology. The world of analog, however, is more highly customized. It also is less easily standardized than the world of digital. This aspect creates unique challenges in supporting an efficient disintegrated supply chain. Recognizing these challenges, the Global Semiconductor Alliance (GSA) has formed the Mixed-Signal/Radio Frequency (RF) Subcommittee.

This subcommittee's work is helping to standardize the interface between many aspects of the analog supply chain. As a result, integrated device manufacturers (IDMs) can more easily and efficiently augment their capabilities by partnering with outside manufacturers and creating environments that support a fab-light or fabless analog industry. The subcommittee helps to link an ecosystem of analog product companies with foundries, electronic design automation (EDA), intellectual property (IP), and other required infrastructure. In doing so, it helps to create an efficient support ecosystem for the analog industry of the future.

The Approach

The first step in tackling this problem is to break the required ecosystem into its primary components. The lifecycle is broken into several phases: design, manufacturing, evaluation, and production. The design phase starts with an idea and ends with a design that's ready for manufacture. In contrast, the manufacturing phase creates the necessary process technology and infrastructure to successfully manufacture the design, therefore enabling an evaluation of the idea. The evaluation and production phases complete the cycle by creating the infrastructure that's needed to evaluate, test, package, and manufacture the product in volume.

The second step is to define the most significant interface points between organizations (internal or across companies) within each phase. It's also necessary to focus efforts on standardizing these points. Interface points were selected and organized within each phase to include design kits, models, IP, maskCAD, process, process control monitoring (PCM), packaging, and test. In each case, a working group has been created to formulate a standard by which information can be properly communicated. These standards are often in the form of checklists with a common vocabulary.

The final step is to fill the teams with a cross-functional group of industry experts that would encompass all facets of the ecosystem. Examples include semiconductor product companies, foundries, EDA vendors, and IP and design-service providers. This common platform could be developed and adopted within all aspects of the supply chain.

While this continues to be a work in progress, good results have been enabled and are in use by many in the industry. The next few sections will describe the objectives, delivered results, and future challenges for the subcommittee's Process Design Kit (PDK), Model, IP, and PCM/Process Checklist Working Groups.

PDK And Model Working Groups

The purpose of the PDK Working Group, which is led by Thomas Moerth of austriamicrosystems, is to establish the basic requirements of mixed-signal (MS)/radio-frequency (RF) design kits. The group also strives to create some standardization around the representation of the kits' content. Together, the member companies in the PDK Working Group (representatives from foundry, fabless, and EDA vendors) determined that a valuable first step would be to have a comprehensive guide to the contents and identify the available components, device types, supported models, and tool compatibility.

The MS/RF PDK Checklist was created and launched in early 2004 and has since been widely adopted. It's quickly becoming a standard document to accompany the release of new versions of MS/RF foundry design kits. The checklist doesn't specify what should be in a PDK. Yet it's clear that the availability of a standard format for representation of its

contents goes a long way toward providing a first-order benchmark for a foundry's customer. The condensed format also provides a first look at process capabilities when trying to determine the most suitable technology for the development of a MS/RF product. In doing so, it frees the customer from having to review a number of different documents in order to identify all available device types and components. The checklist is an incremental but influential first step in standardizing a common set of requirements to get MS/RF designs to market more quickly and efficiently.

The Model Working Group is led by Roberto Tinti of Agilent Technologies. This group has taken a similar approach in addressing the rapidly changing and increasingly intricate requirements of MS/RF modeling. Specifically, it has taken on the task of establishing a modeling checklist, which includes the standard models supported by foundries along with the extensions of those models with features like statistical, mismatch, and noise simulation capabilities.

Designers need to know what types of models are supported by the foundry they're choosing as well as the quality and method of validation of those models. The charter of the Model Working Group is to define the short-term and long-term infrastructure as well as the support needed for MS/RF modeling environments. It goes one level deeper than the PDK Checklist by providing a basis for model comparison, which should assist in the evaluation of suitability and capabilities for MS/RF design. With the release of version 1.2 of the MS/RF SPICE Model Checklist in August 2007, the Model Working Group has delivered an easy-to-read document that greatly helps designers in assessing the model quality of a PDK.

The deliverables of both the PDK and Model Working Groups have been bundled in the latest release (version 2.0) of the PDK Checklist. This version now incorporates the checklist from the Model Working Group, which provides an even more powerful instrument for the customer to compare processes from different foundries. Aside from allowing a comparison of the ingredient list of a design kit, it provides a standardized view of the heart of a PDK and simulation models.

IP Working Group

The IP Working Group is led by David Schwan, engineering manager at RF Micro Devices. This group is intended to address the recognized need for added focus on the key MS/RF IP requirements of semiconductor companies. In contrast to the maturing digital-IP market, the MS/RF IP ecology is still in its infancy. For many reasons, addressing MS/RF IP requirements had previously been considered complex. Examples include the lack of process standardization across foundries, incompatibilities in PDKs and models, and detailed specifications that can be different for each application.

The purpose of the IP Working Group is to outline and communicate the IP requirements for the MS/RF design space including the basic blocks and silicon validation requirements for each. Defining the scope and set of near-term outcomes for this activity provides a foundation for efforts to provide a broader set of standardized IP building blocks. Those blocks, in turn, can be used to accelerate design cycles and lead to a higher level of MS/RF integration (a parallel that can be drawn from the impact of digital IP availability on the development of system-on-a-chip (SoC) designs for digital products). The group's work has been folded into GSA's IPecosystem Tool Suite with the primary contribution being the IP Deliverables Checklist.

PCM/Process Checklist Working Group

The PCM/Process Checklist Working Group is intended to complement the work of existing process roadmaps by helping to standardize the vocabulary, definitions, and key figures of merit for analog and RF technology. The work is subdivided into two initiatives: a process and a PCM checklist. The first initiative hopes to standardize how foundries describe their analog process technologies. In doing so, it will make it easier for them to communicate their analog offerings and help their customers quickly make meaningful comparisons. (The Working Group released its AMS/RF Process Checklist version 1.0 in July 2008.)

The group's second initiative will provide recommendations for the measurements and definitions of the electrical tests used in the monitoring of analog manufactured wafers (often referred to as PCMs). This deliverable hopes to help standardize the communication of analog parametric information about a manufactured wafer between foundry and foundry customers. It will help both parties make the best decisions in creating ever-higher-yielding analog products.

What's Next?

While progress has been made, much work remains in helping to bring order to a custom analog world. The steps described here are helping. However, more will be needed in the coming years to foster standards that help to bridge interface points between organizations, which must increasingly cross company lines.

GSA is helping to provide a forum. But it's up to industry professionals to provide input and participate in the process. Participation allows its members and other industry professionals to hear the views of their customers, partners, competitors, and vendors on a wide variety of topics. This aspect can help to both bring value to their day-to-day activities and foster a better ecosystem for the entire industry.

For more information about GSA's Mixed-Signal/RF Subcommittee and to access the checklists discussed in this article, visit www.gsaglobal.org/subcommittees/msrf/index.asp.

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